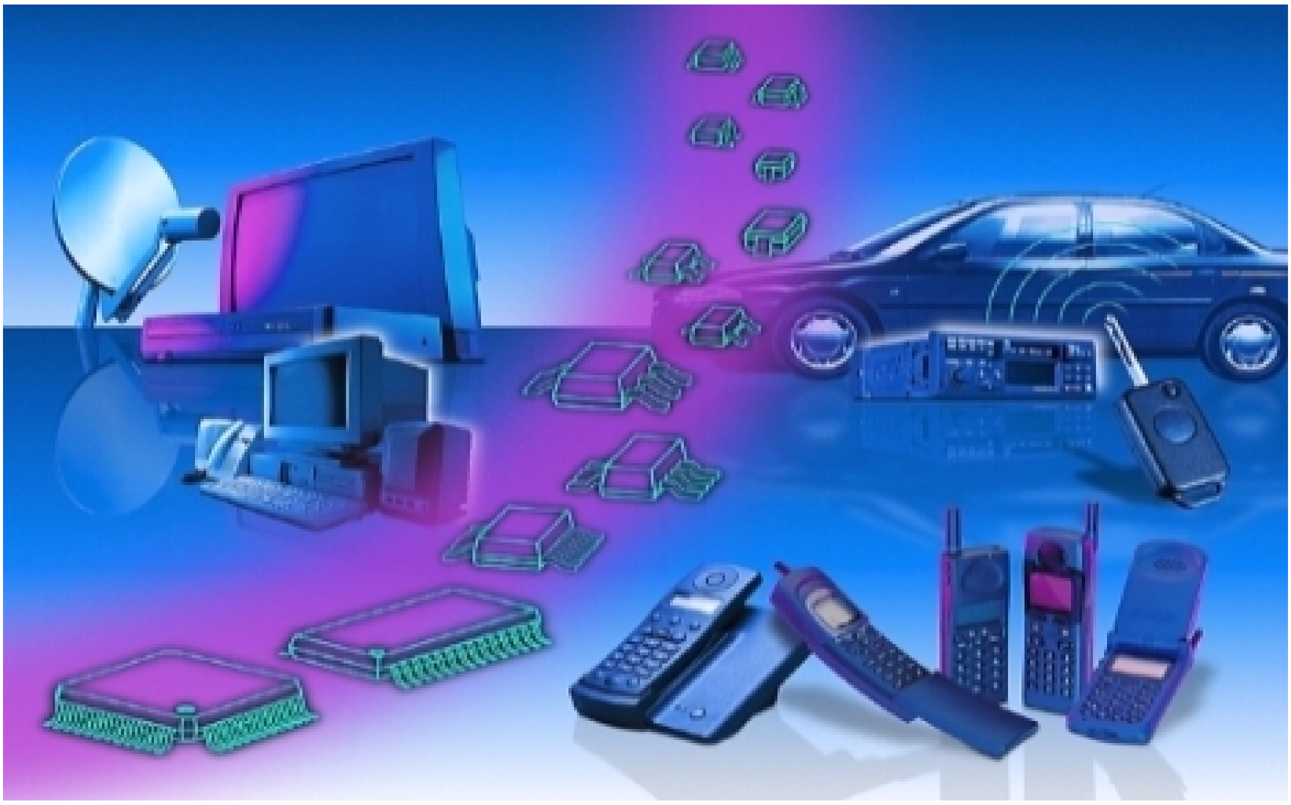

Wireless Components

2 Band TV Tuner Mixer-Oscillator-PLL with unbalanced IF-Amplifier

KTS6027-2, KTS6029-2 Version 2.0

Specification July 2001

Revision History: Current Version: Preliminary Datasheet V 1.1, July 2000		
Previous Version:Target Data Sheet		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
all	all	version to 1.1, status to preliminary
4 - 2	4 - 2	circuit diagram modified
4 - 3	4 - 3	circuit diagram modified
5 - 2	5 - 2	Bus input/output SDA max changed to 6V, Bus input SCL max changed to 6V, ADC input added
5 - 3	5 - 3	new reference for ESD protection
5 - 5	5 - 5	Current consumption for LOW/MID band and HIGH band added, tbf's replaced by data Charge Pump output voltage VCP = 1.3 V min
5 - 8	5 - 8	Oscillator phsase noise -85 dBc/Hz min, -89 dBc/Hz typ
5 - 9	5 - 9	Oscillator phsase noise -85 dBc/Hz min, -89 dBc/Hz typ

Revision History: Current Version: Datasheet, V 2.0, July 2001		
Previous Version:Preliminary Datasheet V 1.1, July 2000		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
all	all	version to 2.0, preliminary deleted
5 - 2	5- 2	definition of thermal properties changed
5 - 5	5 - 5	current consumtion changed

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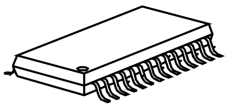
Published by Infineon Technologies AG
Balanstraße 73,
81541 München

Product Info

General Description

The **KTS6027-2/KTS6029-2** is a 5 V mixer/oscillator and synthesizer for analog and digital TV and VCR tuners.

Package



Features

General

- Suitable for analog and digital terrestrial TV tuner
- Compatible with KTS6027-S or KTS6029-S in normal mode
- New features in extended mode
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- single ended IF preamplifier
- 75 Ω output impedance

PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I^2C bus
- 4 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset
- 4 programmable reference divider ratios: 24, 64, 80, 128
- 4 programmable charge pump currents

Application

- The IC is suitable for NTSC tuners in TV- and VCR-sets or CATV set-top receivers for analog and digital (ATSC) TV.

Ordering Information

Type	Ordering Code	Package
KTS6027-2	Q67037-A1162 (tape and reel)	P-TSSOP-28-1
KTS6029-2	Q67037-A1163 (tape and reel)	P-TSSOP-28-1

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 General Description

The **KTS6027-2, KTS6029-2** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV and VCR tuners.

The PLL block with four selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has four output ports. A flag is set when the loop is locked. It can be read by the processor via the I^2C bus.

The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for LOW/MID and HIGH, an IF amplifier, a low-noise reference voltage source, and a band switch.

2.2 Features

General

- Suitable for analog and ATSC TV tuners
- Compatible with KTS6027-S or KTS6029-S in normal mode
- New features in extended mode
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

IF-Amplifier

- single ended IF preamplifier
- 75 Ω output impedance

PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I^2C bus
- 4 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch

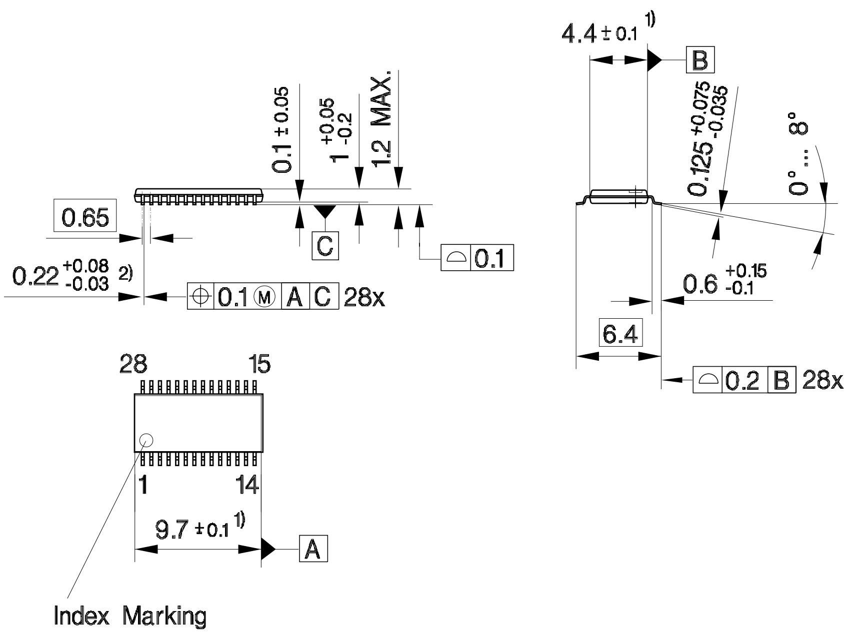
- Lock-in flag
- Power-down reset
- 4 programmable reference divider ratios: 24, 64, 80, 128
- 4 programmable charge pump currents

2.3 Application

- The IC is suitable for NTSC tuners in TV- and VCR-sets or CATV set-top receivers for analog and digital (ATSC) TV.

2.4 Package Outlines

P-TSSOP-28-1



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

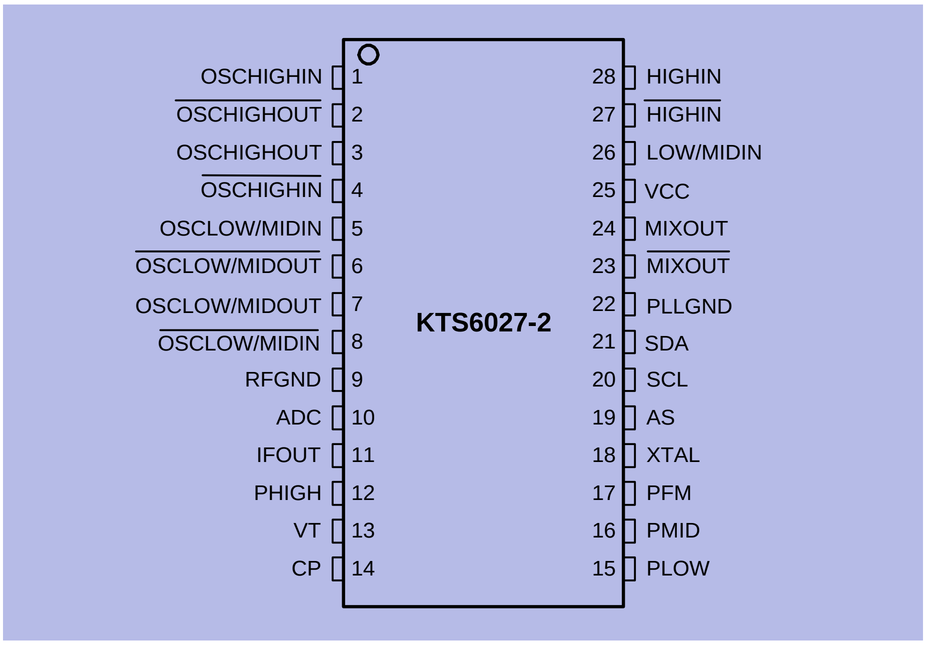


Figure 3-1 KTS6027-2 Pin Configuration

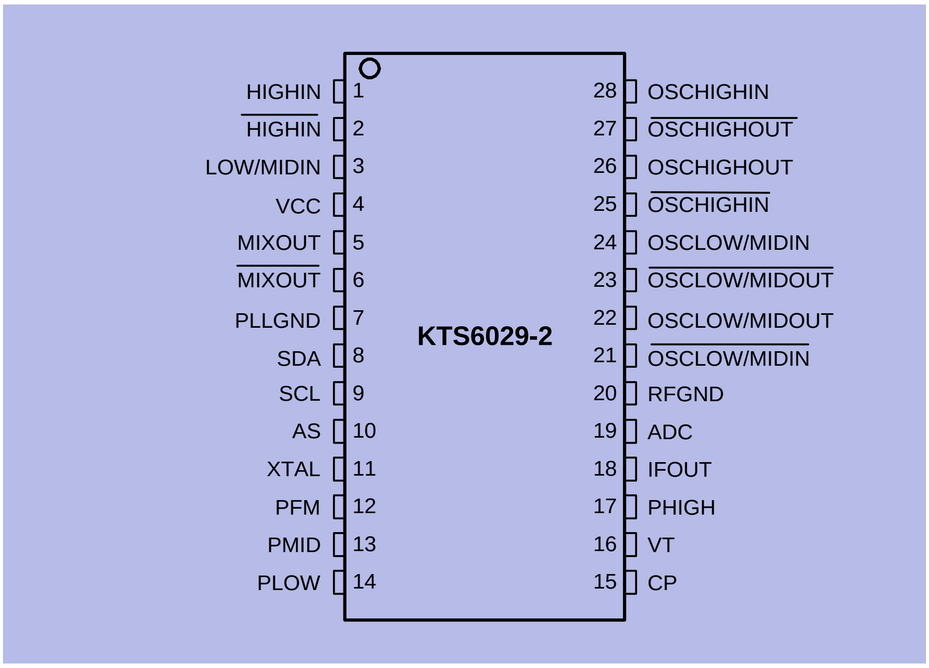


Figure 3-2 KTS6029-2 Pin Configuration

3.2 Internal Pin Configuration

Note: Pin designation refers to KTS6027-2. KTS6029-2 has reversed pinning

Table 3-1 Pin Definition and Function

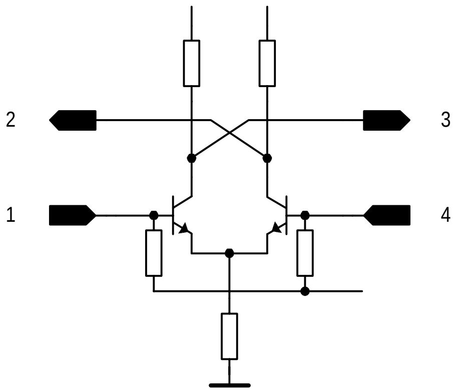
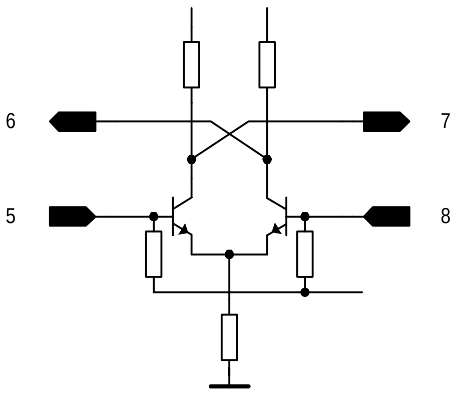
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
1	OSCHIGHIN		0.0 V	1.6 V
2	$\overline{\text{OSC-HIGHOUT}}$		0.0 V	2.8 V
3	OSC-HIGHOUT		0.0 V	2.8 V
4	$\overline{\text{OSCHIGHIN}}$		0.0 V	1.6 V
5	OSCLOW/MIDIN		1.6 V	0.0 V
6	$\overline{\text{OSCLOW/MIDOUT}}$		2.3 V	0.0 V
7	OSCLOW/MIDOUT		2.3 V	0.0 V
8	$\overline{\text{OSCLOW/MIDIN}}$		1.6 V	0.0 V
9	RFGND	analog ground	0.0 V	0.0 V

Table 3-1 Pin Definition and Function (continued)

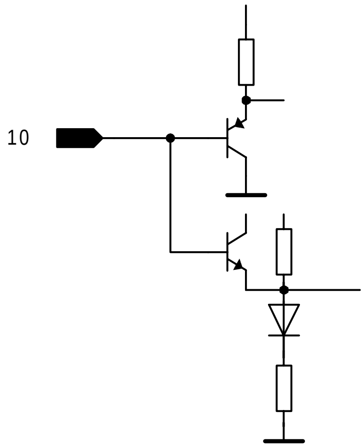
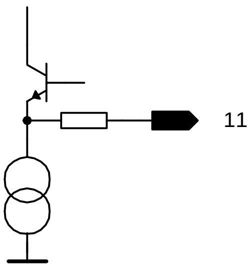
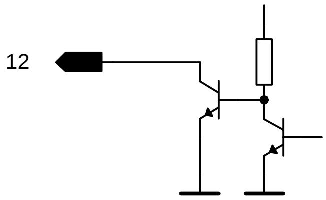
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage LOW/MID	HIGH
10	ADC		V_{ADC}	V_{ADC}
11	IFOUT		2.3 V	2.3 V
12	PHIGH		5.0 V	V_{CE}

Table 3-1 Pin Definition and Function (continued)

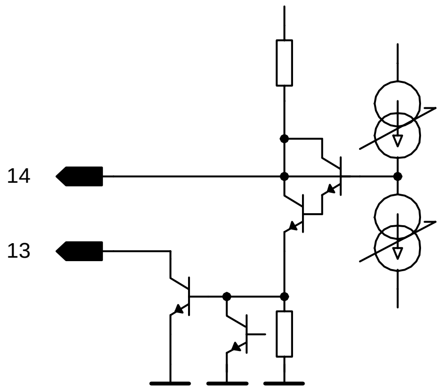
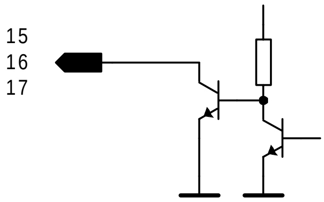
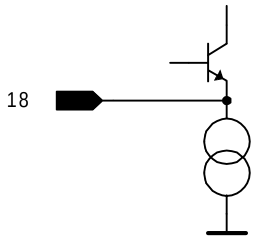
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
13	VT		V_T	V_T
14	CP		2.1 V	2.1 V
15	PLOW		5 V or V_{CE}	5 V
16	PMID		5 V or V_{CE}	5 V
17	PFM		5 V or V_{CE}	5 V or V_{CE}
18	XTAL		3.0 V	3.0 V

Table 3-1 Pin Definition and Function (continued)

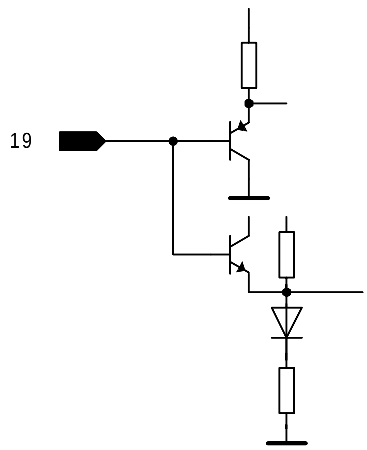
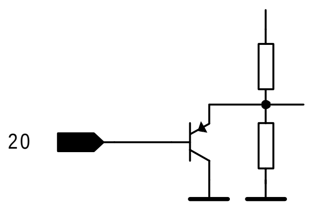
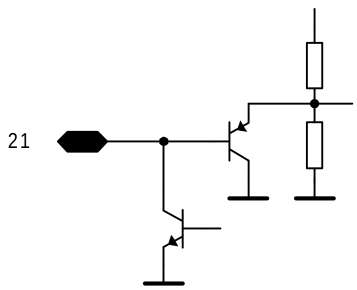
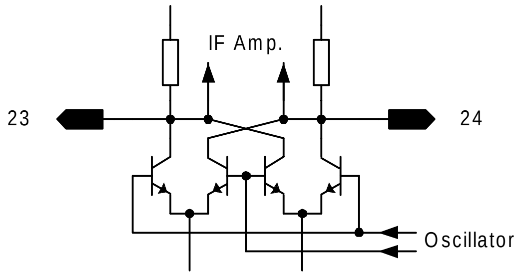
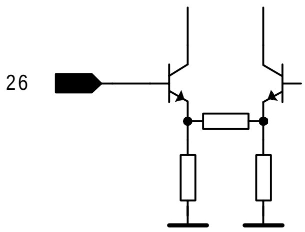
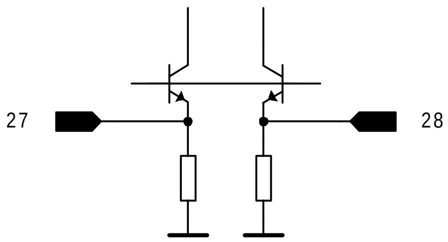
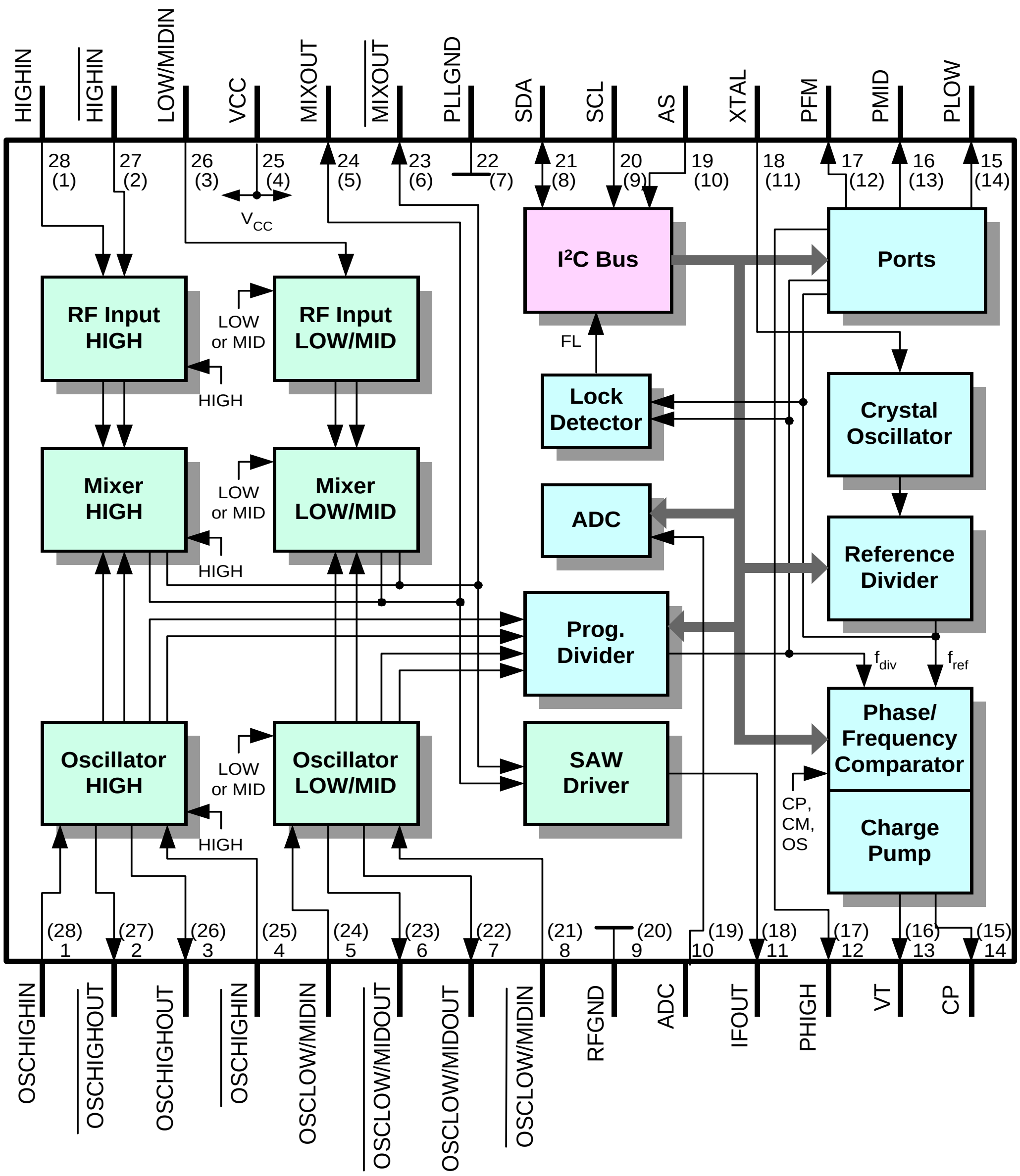
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage LOW/MID	Average DC voltage HIGH
19	AS		V_{AS}	V_{AS}
20	SCL		n.a.	n.a.
21	SDA		n.a.	n.a.
22	PLLGND	digital ground	0.0 V	0.0 V

Table 3-1 Pin Definition and Function (continued)

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage LOW/MID	Average DC voltage HIGH
23	$\overline{\text{MIXOUT}}$		3.8 V	3.8 V
24	MIXOUT		3.8 V	3.8 V
25	VCC	supply voltage	5.0 V	5.0 V
26	LOW/MIDIN		1.8 V	0.0 V
27	$\overline{\text{HIGHIN}}$		0.0 V	0.9 V
28	HIGHIN		0.0 V	0.9 V

3.3 Block Diagram



KTS602729_block_diag

Note: Pin designations in parenthesis refer to KTS6029-2

Figure 3-3 Block Diagram

3.4 Circuit Description

3.4.1 General

In the **normal** mode (see Table 5-7 Test modes on page 32) the IC is compatible with KTS6027-S / KTS6029-S. An **extended** mode makes a reference divider ratio of 24 (see Table 5-8 Reference divider ratio on page 32) and two additional charge pump currents (see Table 5-9 Charge pump current on page 33) available.

3.4.2 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for LOW and / or MID band and HIGH band, an IF amplifier, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of LOW / MID a high-impedance input and in case of HIGH a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive the SAW filter directly.

3.4.3 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency / phase detector to a reference frequency f_{ref} = 31.25, 50, 62.5 or 166.7 kHz.

This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by R = 128, 80, 64 or 24.

The phase detector has two outputs that drive two current sources of opposite polarity as charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits T0 = 1 and T1 = 0. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33 V .

By means of the control bits CP, CM, T0 and T1 the pump current can be switched between four values by software. This programmability permits alteration of the control response time of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports PLOW, PMID, PHIGH and PFM are general-purpose open-collector outputs. The test bits T0 = 0 and T1 = 1 switches the test signals f_{ref} (i.e.f_{XTAL} / 64) and f_{div} (divided input signal) to PLOW and PMID respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is wider than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P (K_{VCO} / f_{XTAL}) (C1+C2) / (C1C2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_{XTAL} the crystal oscillator frequency and C1, C2 the capacitances in the loop filter (see Figure 4-1 KTS6027-2 Evaluation Board on page 20). As the charge pump pulses at i.e. 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

3.4.4 I^2C-Bus Interface

Data is exchanged between the processor and the PLL via the I^2C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C bus.

The data from the processor pass through an I^2C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table "Bit Allocation" (see Table 5-4 Bit Allocation Read / Write on page 31) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin AS (see Table 5-6 Address selection on page 32).

While applying the supply voltage, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when V_{CC} falls below 3.2 V. It will be reset at the end of a READ operation.

4 Applications

Contents of this Chapter

4.1 KTS6027-2 Evaluation Board

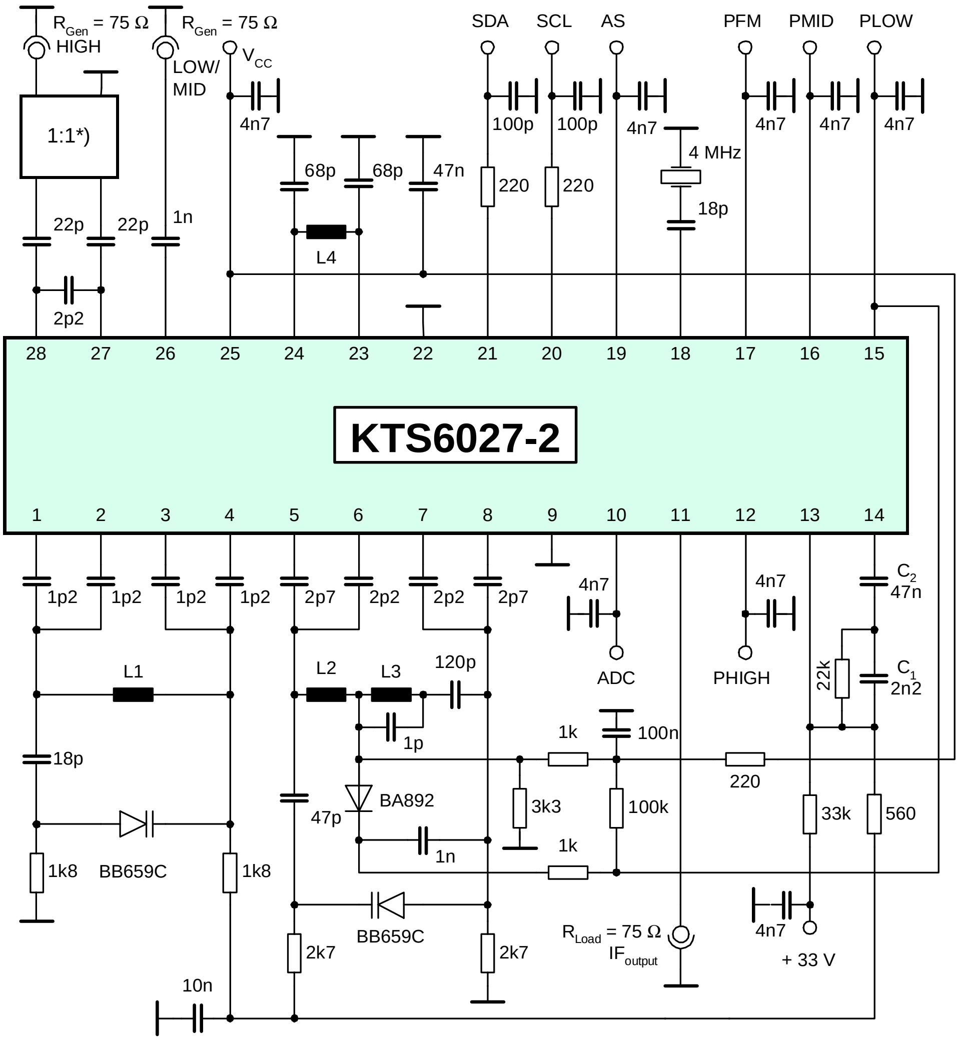


Figure 4-1 KTS6027-2 Evaluation Board (NTSC)

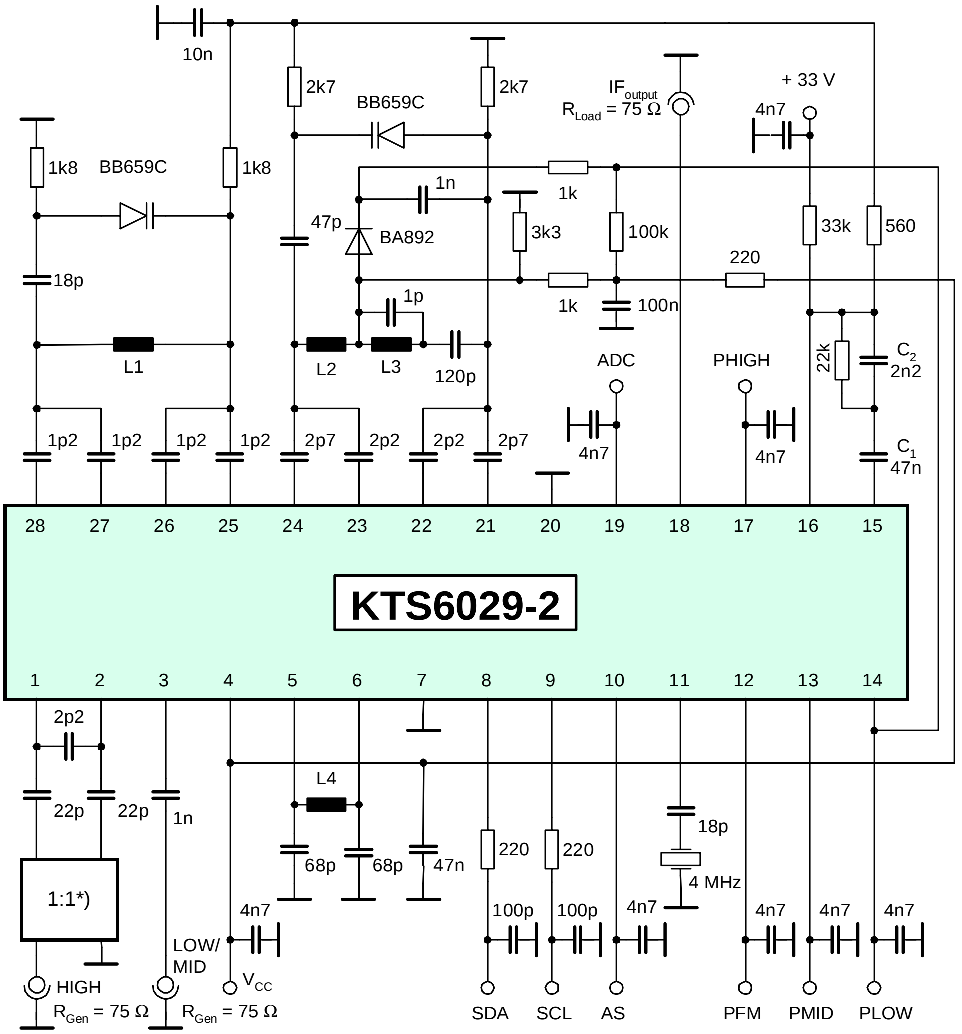
Table 4-1 Recommended band limits in MHz

	RF input		Oscillator	
	min	max	min	max
LOW	55.25	127.25	101	173
MID	133.25	361.25	179	407
HIGH	367.25	803.25	413	849

Table 4-1 Coils

	turns	E	wire E
L1	1.5	2 mm	0.4 mm
L2	3.5	2.5 mm	0.5 mm
L3	9.5	2.5 mm	0.4 mm
L4	12.5	3.5 mm	0.3 mm
*)	TOKO B4F Type 617DB-1023		

4.2 KTS6029-2 Evaluation Board



KTS6029-2 Application Circuit

Figure 4-2 KTS6029-2 Evaluation Board (NTSC)

Table 4-1 Recommended band limits in MHz

	RF input		Oscillator	
	min	max	min	max
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L3	9.5	2.5 mm	0.4 mm
L4	12.5	3.5 mm	0.3 mm
*)	TOKO B4F Type 617DB-1023		

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings

Parameter [1].	Symbol	Limit Values min	Limit Values max	Unit	Remarks
Supply voltage	V_{CC}	-0.3	6	V	
Ambient temperature	T_A	-40	T_{Amax} [2].	°C	
Junction temperature	T_J		+125	°C	
Storage temperature	T_{Stg}	-40	+125	°C	
Temperature difference junction to case [3].	T_{JC}		2	K	
PLL					
CP	V_{CHGPMP}	-0.3	3	V	
	I_{CHGPMP}		1	mA	
Crystal oscillator pin XTAL	V_{XTAL}		V_{CC}	V	
	I_{XTAL}	-5		mA	
Bus input/output SDA	V_{SDA}	-0.3	6	V	
Bus output current SDA	$I_{SDA(L)}$		5	mA	open collector
Bus input SCL	V_{SCL}	-0.3	6	V	
Chip address switch AS	V_{AS}	-0.3	V_{CC}	V	
VCO tuning output (loop filter)	V_T	-0.3	35	V	
ADC input	V_{ADC}	-0.3	V_{CC}	V	
Port outputs PLOW, PMID, PHIGH, PFM	V_P	-0.3	V_{CC}	V	
	$I_{P(L)}$	-1	25	mA	t_{max} = 0.1 sec. at 5.5 V
Total port output current	$\Sigma I_{P(L)}$		40	mA	t_{max} = 0.1 sec. at 5.5 V

Table 5-1 Absolute Maximum Ratings

Parameter [1]	Symbol	Limit Values		Unit	Remarks
		min	max		
Mixer-Oscillator					
Mix input LOW/MID	V_i	-0.3	3	V	
Mix inputs HIGH	V_i		2	V	
	I_i	-5	6	mA	
VCO base voltage	V_B	-0.3	3	V	
VCO collector voltage	V_C		V_{CC}	V	
ESD-Protection [4].					
all pins	V_{ESD}		2	kV	

1). All values are referred to ground (pin), unless stated otherwise.
Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2).The maximum ambient temperature depends on the mounting conditions of the package. Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C. As reference the temperature difference junction to case is given.

3).Referred to top center of package

4). According to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
Supply voltage	V_{CC}	+4.5	+5.5	V			
Programmable divider factor	N	256	32767				
LOW/MID Mixer input frequency range	f_i	40	500	MHz			
HIGH Mixer input frequency range	f_i	350	900	MHz			
LOW/MID Oscillator frequency range	f_O	75	560	MHz			
HIGH Oscillator frequency range	f_O	380	950	MHz			
Ambient temperature	T_A	-20	T_{Amax} 1).	°C			

1).see 5.1.1 Absolute Maximum Ratings on page 2

5.1.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC}

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Supply								
Supply voltage	V_{CC}	4.5	5	5.5	V			
Current consumption	I_{CC}	48	61	74	mA	LOW/MID band		
		51	65	79	mA	HIGH band		
Digital Unit								
PLL								
Crystal oscillator connections XTAL								
Crystal frequency	f_{XTAL}	3.2	4.0	4.8	MHz	series resonance		
Crystal resistance	R_{XTAL}	10		100	Ω	series resonance		
Oscillation frequency	f_{XTAL}	3,99975	4,000	4,00025	MHz	f_{XTAL} = 4 MHz		
Input impedance	Z_{XTAL}	-700	-900	-1100	Ω	f_{XTAL} = 4 MHz		
Charge pump output CP								
Output current, see Table 5-9 Charge pump current on page 12	ICPDH	± 430	± 650	± 860	µA	VCP = 1.8 V		
	ICPH	± 180	± 250	± 360	µA	VCP = 1.8 V		
	ICPDL	± 90	± 125	± 180	µA	VCP = 1.8 V		
	ICPL	± 35	± 50	± 70	µA	VCP = 1.8 V		
Tristate current	ICPZ		± 1		nA	T0=1, T1=0		
Output voltage	VCP	1.3		2.5	V	PLL locked		
Drive output VT (open collector)								
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = 1, T1 = 0		
LOW output voltage	V_{TL}			0.5	V	I_{TL} = 1.0 mA		
I^2C-Bus								
Bus inputs SCL, SDA								
HIGH input voltage	V_{IH}	3		5.5	V			
LOW input voltage	V_{IL}	0		1.5	V			
HIGH input current	I_{IH}			10	µA	$V_{IH} = V_{CC}$		
LOW input current	I_{IL}	-10			µA	V_{IL} = 0 V		

Table 5-3 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Bus output SDA (open collector)								
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V		
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA		
Edge speed SCL,SDA								
Rise time	t_r			300	ns			
Fall time	t_f			300	ns			
Clock timing SCL								
Frequency	f_{SCL}	0		400	kHz			
HIGH pulse width	t_H	0.6			µs			
LOW pulse width	t_L	1.3			µs			
Start condition								
Set-up time	t_{susta}	0.6			µs			
Hold time	t_{hsta}	0.6			µs			
Stop condition								
Set up time	t_{susto}	0.6			µs			
Bus free	t_{buf}	1.3			µs			
Data transfer								
Set-up time	t_{sudat}	0.1			µs			
Hold time	t_{hdat}	0			µs			
Input hysteresis SCL, SDA	V_{hys}		200		mV			
Pulse width of spikes which are suppressed	t_{sp}	0		50	ns			
Capacitive load for each bus line	C_L			400	pF			
Port outputs PLOW, PMID, PHIGH, PFM (open collector)								
HIGH output current	I_{POH}			1	µA	V_{POH} = 5 V		
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 25 mA		
ADC port input								
HIGH input current	I_{ADCH}			10	µA			
LOW input current	I_{ADCL}	-10			µA			
Address selection input AS								
HIGH input current	I_{ASH}			50	µA	V_{ASH} = 5 V		
LOW input current	I_{ASL}	-50			µA	V_{ASL} = 0 V		

Table 5-3 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Analog Unit								
LOW/MID Band Section (including IF amplifier)								
Voltage gain	G_V	15	18	21	dB	f_{RF} = 55.25 to 361.25 MHz, f_{IF} = 41,25 to 58.75 MHz		
Mixer noise figure	NF		9	11	dB	f_{RF} = 55.25 to 361.25 MHz		
Output voltage causing 0.8 % of crossmodulation in channel, see 5.4.6 on page 17	V_o		109		dBµV	f_{RFw} = 55.25 MHz		
	V_o		109		dBµV	f_{RFw} = 361.25 MHz		
Input IP2	IP2		140		dBµV	f_{RF1} = 55.25 MHz f_{RF2} = 111.00 MHz, P_{RF1} = P_{RF2}		
	IP2		135		dBµV	f_{RF1} = 361.25 MHz f_{RF2} = 723.00 MHz, P_{RF1} = P_{RF2}		
Input IP3	IP3		110		dBµV	f_{RF1} = 55.25 MHz f_{RF2} = 60.75 MHz, f_{RF2} = 61.75 MHz, P_{RF1} = P_{RF2} = P_{RF3}		
	IP3		110		dBµV	f_{RF1} = 253.25 MHz f_{RF2} = 258.75 MHz, f_{RF2} = 259.75 MHz, P_{RF1} = P_{RF2} = P_{RF3}		
Output voltage causing 1 dB compression	Vo		115		dBµV	f_{RF} = 55.25 MHz		
	Vo		115		dBµV	f_{RF} = 361.25 MHz		
Mixer input impedance	R_i	0.5	1	1.5	kΩ	parallel equivalent circuit, f_{RF} = 100 MHz		
	C_i		2	3	pF	parallel equivalent circuit, f_{RF} = 100 MHz		
Oscillator frequency shift, PLL unlocked	$\Delta f_{Osc(V)}$			400	kHz	V_{CC} = 5 V ± 10 %		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(T)}$			500	kHz	ΔT = 25 °C		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(t)}$			100	kHz	t = 5 s up to 15 min after switching on		

Table 5-3 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Oscillator pulling, PLL unlocked	V_i	100	108		dBµV	Δf = 10 kHz f_{RF} = 55.25 MHz		
	V_i	100	108		dBµV	Δf = 10 kHz f_{RF} = 361.25 MHz		
Oscillator phase noise [1)].	Φ_{OSC}	-86	-89		dBc/Hz	fm = 10kHz		
IF suppression	a_{IF}	15	20		dB	V_i = 80 dBµV		
HIGH Band Section (including IF amplifier)								
Voltage gain	G_V	26	29	32	dB	f_{RF} = 367.25 MHz to 801.25 MHz, f_{IF} = 41,25 to 58.75 MHz		
Mixer noise figure	NF		6	9	dB	f_{RF} = 367.25 to 613.25 MHz		
			7	10	dB	f_{RF} = 619.25 to 801.25 MHz		
Output voltage causing 0.8 % of crossmodulation in channel, see 5.4.7 on page 18	V_o		109		dBµV	f_{RFw} = 403.25 MHz		
	V_o		109		dBµV	f_{RFw} = 775.25 MHz		
Input IP2	IP2		130		dBµV	f_{RF1} = 373.25 MHz f_{RF2} = 747.00 MHz, $P_{RF1} = P_{RF2}$		
Input IP3	IP3		99		dBµV	f_{RF1} = 503.25 MHz f_{RF2} = 510.25 MHz, f_{RF2} = 512.25 MHz, $P_{RF1} = P_{RF2} = P_{RF3}$		
	IP3		99		dBµV	f_{RF1} = 775.25 MHz f_{RF2} = 780.75 MHz, f_{RF2} = 781.75 MHz, $P_{RF1} = P_{RF2} = P_{RF3}$		
Output voltage causing 1 dB compression	Vo		115		dBµV	f_{RF} = 503.25 MHz		
	Vo		115		dBµV	f_{RF} = 799.25 MHz		
Mixer input impedance	R_i	14	20	26	Ω	serial equivalent circuit, f_{RF} = 600 MHz		
	L_i	6	10	14	nH	serial equivalent circuit, f_{RF} = 600 MHz		
Oscillator frequency shift, PLL unlocked	$\Delta f_{Osc(V)}$			400	kHz	V_{CC} = 5 V ± 10 %		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(T)}$			800	kHz	ΔT = 25 °C		

Table 5-3 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(t)}$			100	kHz	t = 5 s up to 15 min after switching on		
Oscillator pulling, PLL unlocked	V_i	100	108		dBµV	Δf = 10 kHz f_{RF} = 367.25 MHz		
		100	108		dBµV	Δf = 10 kHz f_{RF} = 801.25 MHz		
Oscillator phase noise [1)]		-86	-89		dBc/Hz	fm = 10kHz		
IF suppression	a_{IF}	15	20		dB	V_i = 80 dBµV		
SAW preamplifier								
IF output impedance	R_{IF}			80	Ω	serial equivalent circuit, f_{IF} = 45.75 MHz		
	L_{IF}		7		nH			
Rejection at the IF outputs								
Divider interference rejection [2).]	Vo			30	dBµV			
Channel CH6 beat [3).]	INT_{CH6}	70			dBc	V_{RFpix} = 80 dBµV V_{RFsnd} = 80 dBµV		
Channel A-5 beat rejection [4).]	INT_{CHA5}	70			dBc	V_{RFpix} = 80 dBµV		

■ This value is only guaranteed in lab.

1). Measured in the evaluation board. (see Chapter 4)

2). This is the level of divider interferences close to the IF frequency. For example channel S3: fOSC = 158.15 MHz, 1/4 fOSC = 39.5375 MHz. Measured in the evaluation board. (see Chapter 4)

3). Channel 6 beat is the interfering product of f_{RFpix} + f_{RFsnd} - f_{OSC} of channel 6 at 42 MHz. Measured in the evaluation board. (see Chapter 4)

4). Channel A-5 beat is the interfering product of f_{RFPIX} + f_{RFSND} - f_{OSC} of channel A-5, f_{beat} = 45.5 MHz. The possible mechanisms are f_{OSC} - 2 x f_{IF} or 2 x f_{RFpix} - f_{OSC}. Measured in the evaluation board. (see Chapter 4)

5.2 Programming

Table 5-4 Bit Allocation Read / Write

Byte	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB	Ack
Write Data									
Address Byte	1	1	0	0	0	MA1	MA0	0	A
Progr. Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	A
Progr. Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte	1	CP	T1	T0	CM	RSA	RSB	OS	A
Bandswitch Byte [1].	x	x	x	x	P3	P2	P1	P0	A
Read Data									
Address Byte	1	1	0	0	0	MA1	MA0	1	A
Status Byte	POR	FL	x	x	x	A2	A1	A0	A

1). see Table 5-10 Bandswitching on page 12

Table 5-5 Description of symbols

Symbol	Description
MA0, MA1	Address selection bits (see Table 5-6 Address selection on page 11)
N14 to N0	programmable divider bits: $N = 2^{14} \times N14 + 2^{13} \times N13 + \ldots + 2^{3} \times N3 + 2^{2} \times N2 + 2^{1} \times N1 + N0$
CP	charge pump current: bit = 0: charge pump current = 50 µA bit = 1: charge pump current = 250µA
T1, T0	test bits (see Table 5-7 Test modes on page 11)
CM	charge pump mode bit (see Table 5-9 Charge pump current on page 12)
RSA, RSB	reference divider bits (see Table 5-8 Reference divider ratio on page 11)
OS	tuning amplifier control bit: bit = 0: enable V_T bit = 1: disable V_T
PLOW, PMID, PHIGH, PFM, see 5-10 on page 12	NPN ports control bits: bit = 0: NPN open-collector output is inactive bit = 1: NPN open-collector output is active
A0, A1, A2	ADC bits (see Table 5-11 A/D converter levels on page 13)
FL	PLL lock flag bit = 1: loop is locked
POR	Power-on reset flag flag is set at power-on and reset at the end of READ operation
x	don‘t care

Table 5-6 Address selection

Voltage at AS	MA1	MA0
(0...0.1) * V_{CC}	0	0
(0.2...0.3) * VCC or open circuit	0	1
(0.4...0.6) * V_{CC}	1	0
(0.9...1) * V_{CC}	1	1

Table 5-7 Test modes

Test mode	Mode	T1	T0
Normal operation	normal [1]	0	0
Charge pump output, CP is in high-impedance state		0	1
PMID = fdiv output, PLOW = fref output		1	0
Extended operation	extended	1	1

1). In this mode the IC is compatible with KTS6027-S / KTS6029-S

Table 5-8 Reference divider ratio

Reference divider ratio	Mode [1]	T1	T0	RSA	RSB	fref [2]
80	normal	0	0	x	0	50 kHz
		0	1			
		1	0			
128		0	0	0	1	31.25 kHz
		0	1			
		1	0			
64		0	0	1	1	62.5 kHz
		0	1			
		1	0			
80	extended	1	1	0	0	50 kHz
128				0	1	31.25 kHz
24				1	0	166.7 kHz
64				1	1	62.5 kHz

1). see Table 5-7 Test modes on page 11

2). With a 4 MHz quartz.

Table 5-9 Charge pump current

Charge pump current	Mode [1]	CP	T1	T0	CM
50 µA	normal	0	0	0	x
250 µA		1			x
50 µA	extended	0	1	1	0
125 µA		0			1
250 µA		1			0
600 µA		1			1

1). see Table 5-7 Test modes on page 11

Table 5-10 Bandswitching

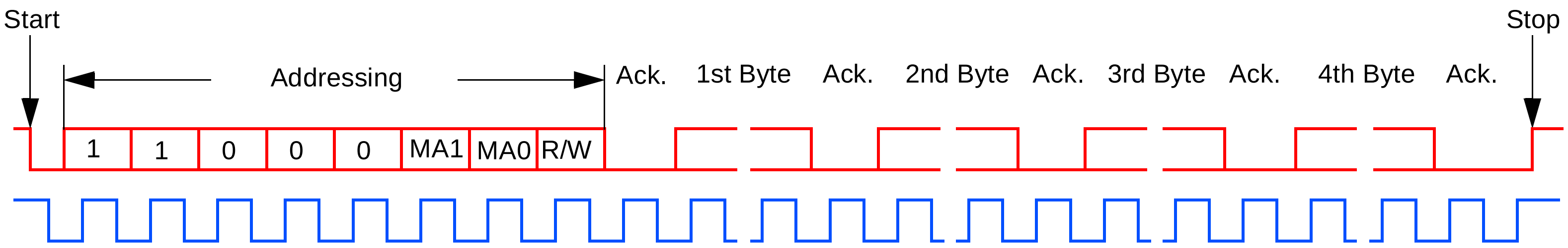
Bit Designation		P3	P2	P1	P0
Active Port	**Pin**				
PHIGH [1]	12	0	0	0	0
PLOW	15	0	0	0	1
PMID	16	0	0	1	0
not used		0	0	1	1
PHIGH	12	0	1	0	0
PLOW, PFM	15, 17	0	1	0	1
PMID, PFM	16, 17	0	1	1	0
not used		0	1	1	1
PHIGH	12	1	0	0	0
PLOW, PFM	15, 17	1	0	0	1
PMID, PFM	16, 17	1	0	1	0
not used		1	0	1	1
PHIGH, PFM	12, 17	1	1	0	0
PLOW, PFM	15, 17	1	1	0	1
PMID, PFM	16, 17	1	1	1	0
not used		1	1	1	1

1). Default after power-on

Table 5-11 A/D converter levels

Voltage at ADC	A2	A1	A0
$(0...0.15)*V_{CC}$	0	0	0
$(0.15...0.3)*V_{CC}$	0	0	1
$(0.3...0.45)*V_{CC}$	0	1	0
$(0.45...0.6)*V_{CC}$	0	1	1
$(0.6...1)*V_{CC}$	1	0	0

5.3 I^2C Bus Timing Diagram



Telegram examples:

Start-ADB-DB1-DB2-CB-BB-Stop

Start-ADB-CB-BB-DB1-DB2-Stop

Start-ADB-DB1-DB2-Stop

Start-ADB-CB-BB-Stop

Abbreviations:

Start= start condition

ADB= address byte

DB1= prog. divider byte 1

DB2= prog. divider byte 2

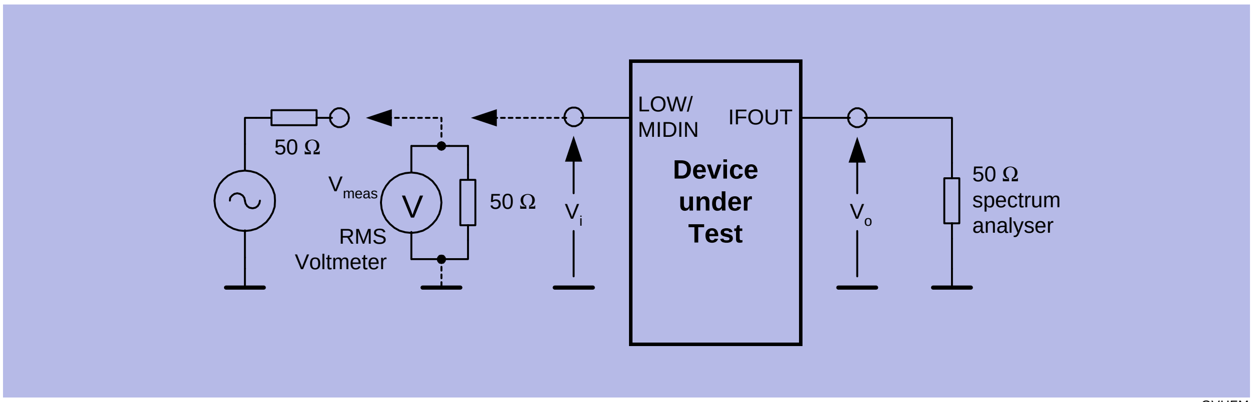
CB= Control byte

BB= Bandswitch byte

Stop= stop condition

5.4 Test Circuits

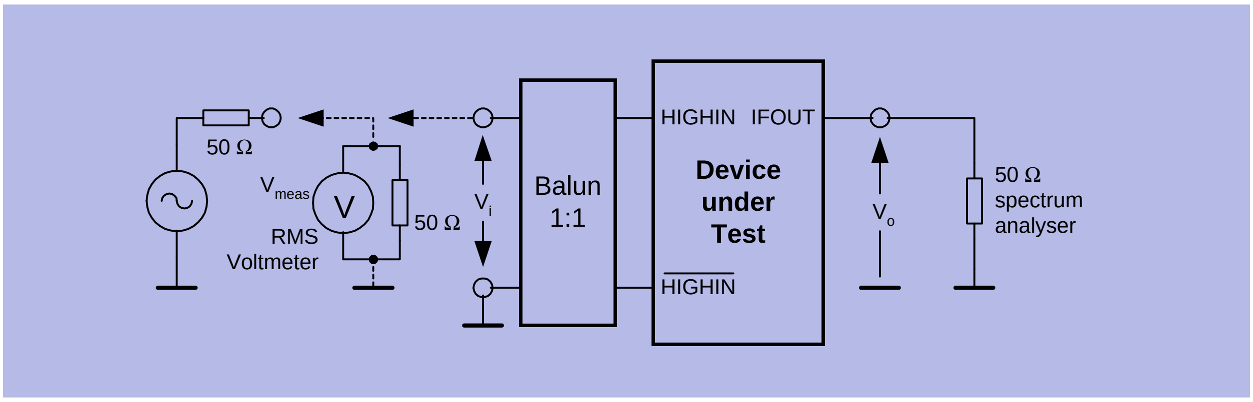
5.4.1 Gain (G_V) test Set-up in LOW/MID



GVHFM

- Z_i >> 50 Ω => V_i = 2 x V_{meas} = 80 dBµV
- V_i = V_{meas} + 6dB = 80 dBµV
- G_v = 20 log(V_0 / V_i)

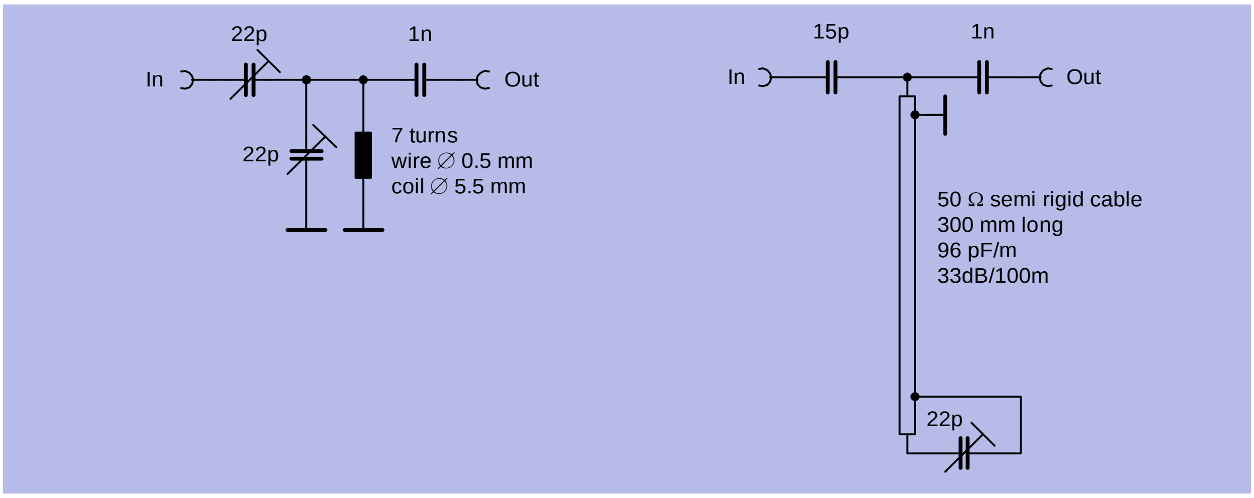
5.4.2 Gain (G_V) test Set-up in HIGH



GUHFM

- V_i = V_{meas} = 70 dBµV
- G_v = 20 log(V_0 / V_i) + 1 dB (1 dB = insertion loss of balun)

5.4.3 Matching circuit for optimum noise figure in LOW/MID



NFM

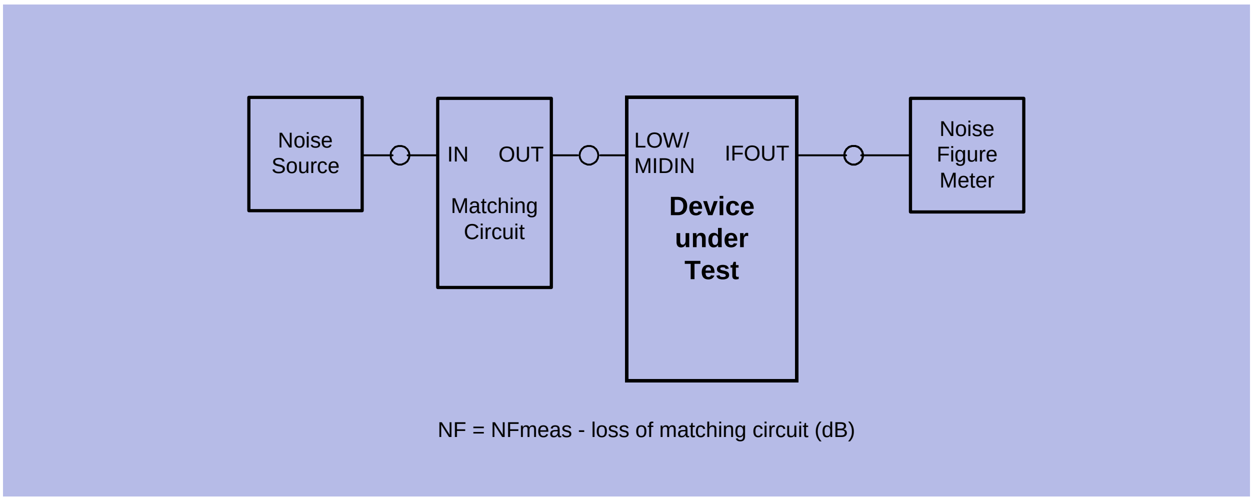
For f_{RF} = 50 MHz

- loss = 0 dB
- image suppression = 16 dB

For f_{RF} = 150 MHz

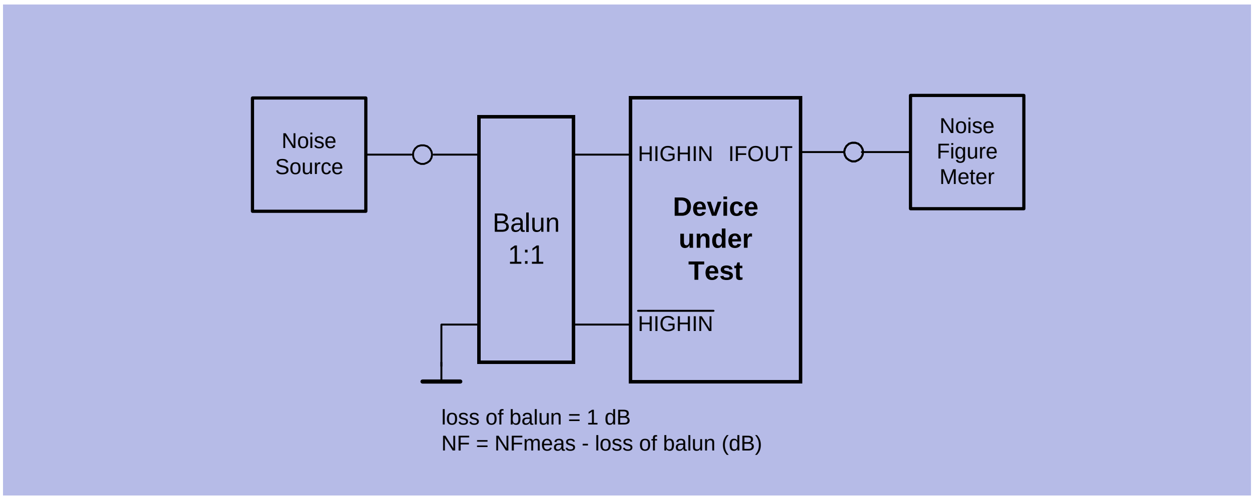
- loss = 1.3 dB
- image suppression = 13 dB

5.4.4 Noise Figure Test Set-up in LOW/MID



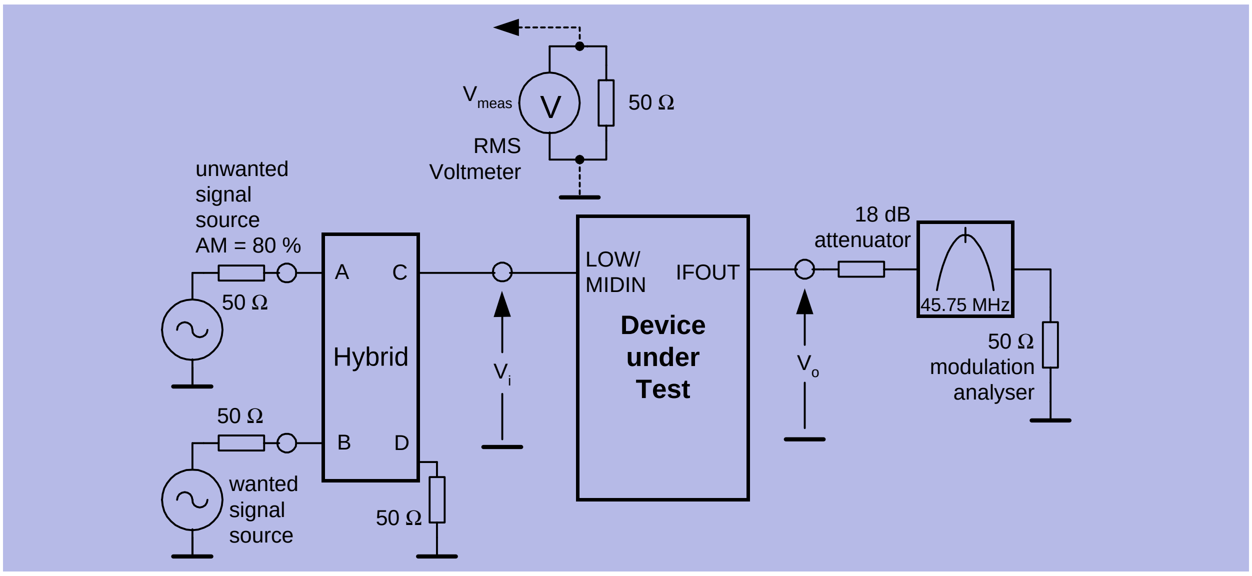
NFVHFM

5.4.5 Noise Figure Test Set-up in HIGH



NFUHFM

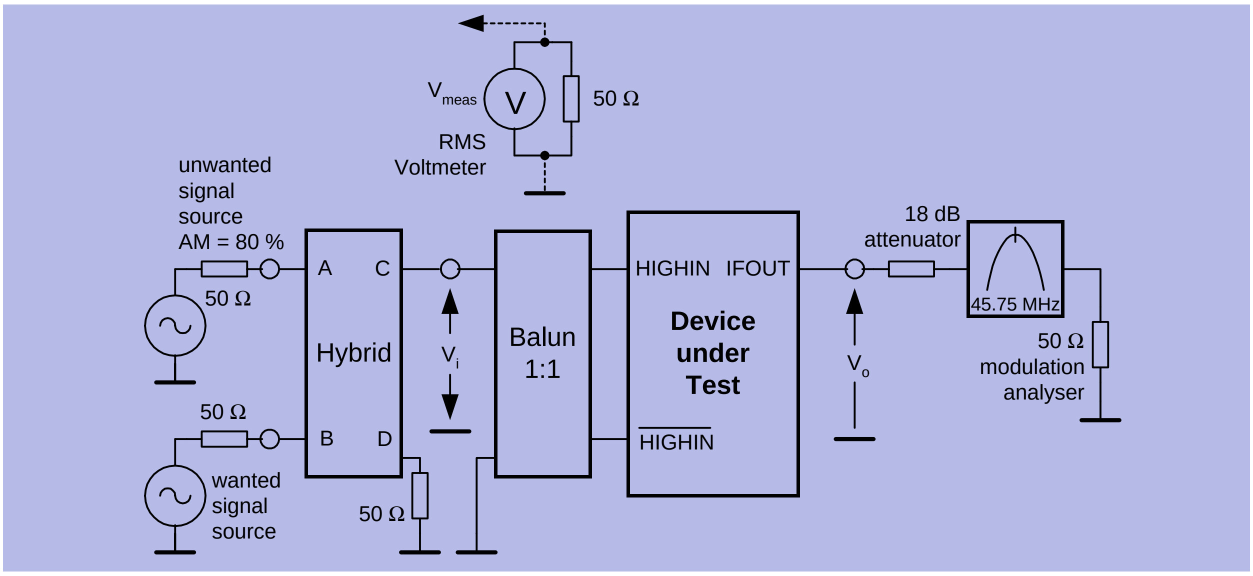
5.4.6 Cross modulation Test Set-up in LOW/MID band



XVHFM

- $Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas}$
- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd} , 80 % AM modulated with 1 kHz

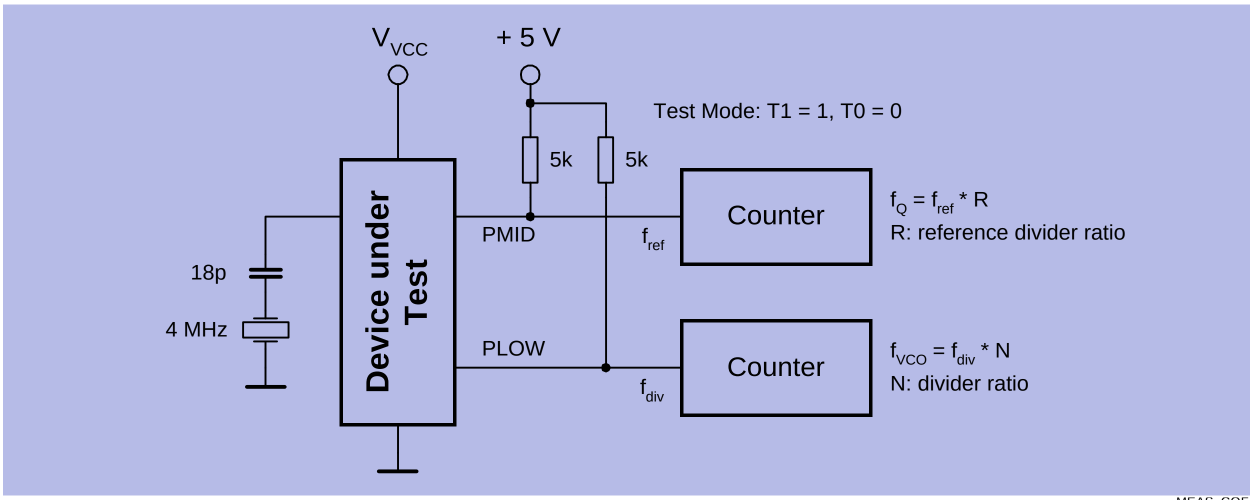
5.4.7 Cross modulation Test Set-up in HIGH band



XUHFM

- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd} , 80 % AM modulated with 1 kHz

5.4.8 Measurement of f_{ref} and f_{div}

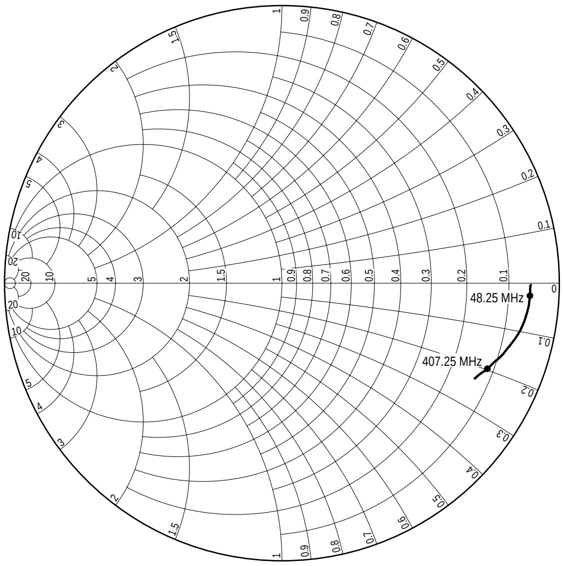


MEAS_COF

5.5 Electrical Diagrams

5.5.1 Input admittance (S11) of the LOW/MID band mixer input

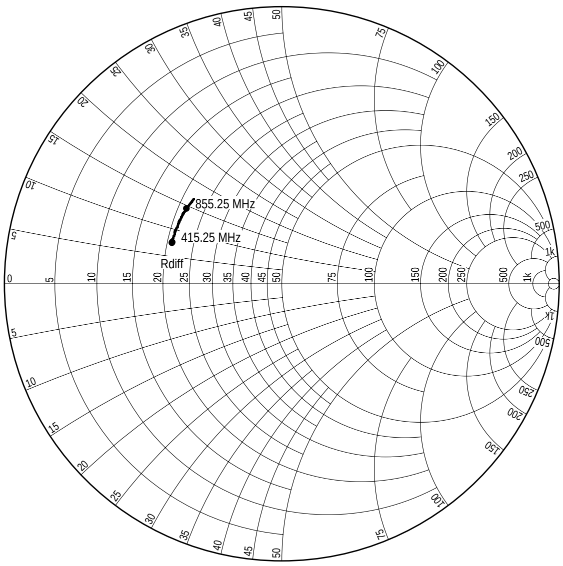
Y_0 = 20mS



Y_VHFMIX

5.5.2 Input impedance (S11) of the HIGH band mixer input

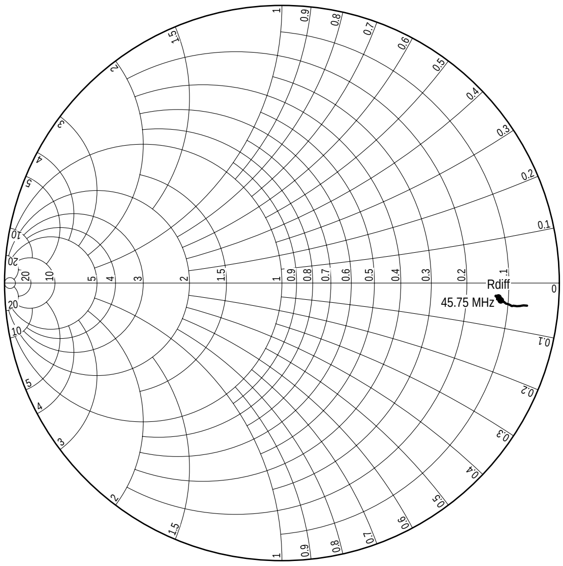
Z_0 = 50 Ω (symmetrical)



Zn_UHFMIX

5.5.3 Output admittance (S22) of the Mixer output

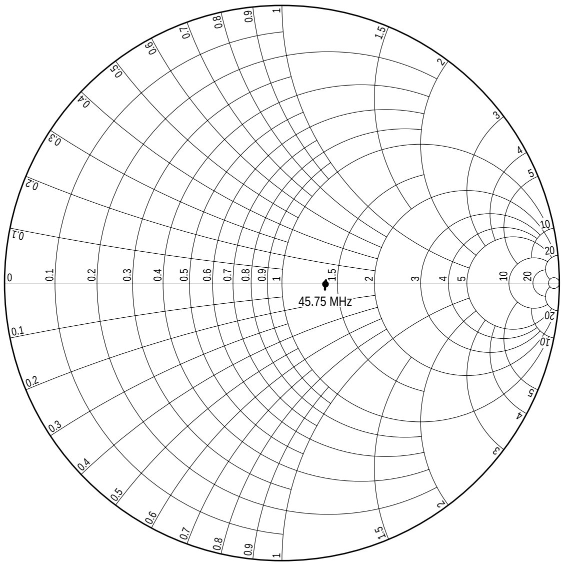
Y_0 = 20mS



Y_MIXOUT

5.5.4 Output impedance (S22) of the IF output

Z_0 = 50 Ω



UIFOUT